module p5(A, M);

output A;

input[2:0] M;

and and0 (a0\_out, M[0], M[1]);

and and1 (a1\_out, M[1], M[2]);

and and2 (a2\_out, M[2], M[0]);

or out(A, a0\_out,a1\_out,a2\_out);

endmodule

module tb\_p5();

reg[2:0] M;

wire A;

integer i;

p5 UUT(A,M);

initial

begin

$monitor("M = %b", M, ", A = ", A);

for ( i=0; i<=7; i=i+1)

begin

M=i;

#10

$display("\n\n");

end

end

endmodule

